

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A semiconductor module with a configuration for the self-test of a plurality of bidirectionally operating interface circuits, comprising:

first and second equally sized groups of interface circuits, wherein each interface circuit of said first group is assigned exactly one interface circuit of said second group;

a respective electrical connection of the interface circuits of said first and second groups to an outside of the semiconductor module, for enabling a self-test;

a first circuit connected to said first group and serving to generate test signals to be multiplexed in and output via said interface circuits of said first group;

a second circuit connected to said second group for receiving and processing test signals received via said interface circuits of said second group; and

a respective separate voltage supply for said first and second groups of interface circuits.

Applic. No. 10/075,656

Response Dated June 9, 2005

Responsive to Office Action of March 9, 2005

Claim 2 (previously presented). The semiconductor module according to claim 1, which further comprises

a third circuit connected to said second group and serving to generate test signals to be multiplexed in and output via said interface circuits of said second group; and

wherein said second circuit is connected to said first group for receiving and processing test signals received via said interface circuits of said first group.

Claim 3 (original). The semiconductor module according to claim 1, wherein said circuit for generating test signals includes a pseudorandom number generator.

Claim 4 (original). The semiconductor module according to claim 1, wherein said circuit for generating test signals includes a linear feedback shift register.

Claim 5 (original). The semiconductor module according to claim 1, wherein said circuit for receiving and processing test signals includes a circuit for calculating a signature from the test signals.

Applic. No. 10/075,656

Response Dated June 9, 2005

Responsive to Office Action of March 9, 2005

Claim 6 (original). The semiconductor module according to claim 1, wherein said circuit for receiving and processing test signals includes a multiple input shift register.

Claim 7 (original). A self-test method, which comprises the following steps:

providing a semiconductor module according to claim 1 and testing the bidirectionally operating interface circuits of the semiconductor module by

connecting the assigned interface circuits of the first and second groups of interface circuits outside the module;

supplying the two groups of interface circuits with a separate supply voltage;

generating test signals, coupling in the test signals, and outputting the test signals via the first group of interface circuits;

receiving the test signals via the second group of interface circuits; and

comparing the received test signals with prescribed values for fault-free functioning of the interface circuits.

Applic. No. 10/075,656

Response Dated June 9, 2005

Responsive to Office Action of March 9, 2005

Claim 8 (original). The method according to claim 7, which comprises:

after processing the test signals output by the first group and received by the second group of interface circuits, reversing a test direction,

such that the test signals generated by the circuit that interacts with the second group are output via the second group of interface circuits and are received via the first group of interface circuits; and receiving and comparing test signals with prescribed values for fault-free functioning of the interface circuits.

Claim 9 (original). The method according to claim 7, which comprises generating test signals with pseudorandom distribution, calculating a signature from the received test signals, and comparing the signature with a prescribed signature for fault-free functioning of the interface circuits.

Claim 10 (original). The method according to claim 7, which comprises influencing a connection of the assigned interface circuits in order to include an influence of interference quantities in the self-test.

Applic. No. 10/075,656

Response Dated June 9, 2005

Responsive to Office Action of March 9, 2005

Claim 11 (previously presented). The method according to claim 10, wherein the influencing step comprises selecting an influence from a group consisting of resistive, capacitive, and inductive influences.

Claim 12 (original). The method according to claim 7, which comprises modulating low-frequency signal voltages onto at least one of the supply voltages of the interface groups.

Claim 13 (original). The method according to claim 12, which comprises modulating two low-frequency sinusoidal signals of different frequency onto both supply voltages.